

### **REMARKS/ARGUMENTS**

This paper is being provided in response to the Office Action dated December 29, 2005, for the above-referenced application. In this response, Applicant has removed text from the specification and amended Claims 1 and 6 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the changes to the specification do not add new matter and that the amendments to the claims are fully supported by the originally-filed specification.

In response to the objection to the text added to page 12, line 9 of the specification, in Applicant's amendment filed on May 9, 2005, Applicant has modified the specification herein to remove the portion of text that is the basis for this objection. Accordingly, Applicant respectfully requests that the objection be reconsidered and withdrawn.

In response to the rejection of Claims 1, 5-7, 11 and 20-23 under 35 U.S.C. 112, first paragraph, Applicant has amended independent Claims 1 and 6 to remove that portion of the claims cited in the Office Action as the basis for this rejection. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 1 and 6 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,545,575 to Cheng et al. (hereinafter "Cheng") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent Claim 1, as amended herein, recite a semiconductor device that includes a semiconductor substrate and an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricated. A gate electrode is formed on the semiconductor substrate. The gate electrode and the insulating film define at least one lightly doped first drain and source diffusion layer. At least one sidewall covers said gate electrode therewith. At least one heavily doped second drain and source diffusion layer is formed at a surface of the semiconductor substrate around the gate electrode. The at least one lightly doped first drain and source diffusion layer contacts the at least one heavily doped second drain and source diffusion layer on at least a bottom and a lateral side. The at least one sidewall has connected thereto a sidewall offset extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one of regions below which the at least one heavily doped second drain and source diffusion layer is to be formed. The sidewall offset has a lateral dimension extending along a lateral surface of a gate oxide film on which the gate electrode is formed by an amount that is greater than a thickness of the sidewall. The at least one lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the at least one heavily doped second drain and source diffusion layer extends below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along the surface of the semiconductor substrate. The at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer.

Independent claim 6, as amended herein, recites a semiconductor device including a semiconductor substrate and an insulating film formed at a surface of the semiconductor substrate for defining device regions in each of which a semiconductor device is to be fabricate. A gate electrode is formed on the semiconductor substrate. The gate electrode and the insulating film define at least one lightly doped first drain and source diffusion layer. At least one sidewall covers the gate electrode therewith. At least one heavily doped second drain and source diffusion layer is formed at a surface of said semiconductor substrate around the gate electrode. The at least one lightly doped first drain and source diffusion layer contacts the at least one heavily doped second drain and source diffusion layer on at least a bottom and a lateral side. The at least one sidewall has connected thereto a sidewall offset extending outwardly of the gate electrode along the surface of the semiconductor substrate in at least one of regions below which the at least one heavily doped second drain and source diffusion layer is formed. The sidewall offset extends along a lateral surface of a gate oxide film on which the gate electrode is formed by an amount that is greater than a thickness of said sidewall. Low-resistive wiring layers are formed at surfaces of the drain and source diffusion layers. The low-resistive wiring layers are located outwardly beyond a peripheral edge of at least one of the sidewall and the sidewall offset in the at least one of said drain and source diffusion layer. The at least one lightly doped first drain and source diffusion layer extends towards the gate electrode beyond an edge of the sidewall offset, and the at least one heavily doped second drain and source diffusion layer extend below the sidewall offset but spaced outwardly away from an edge of the gate electrode in a direction along the surface of the semiconductor substrate. The at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer

edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer.

The Cheng reference discloses an insulated gate semiconductor device having gate electrodes, and a source region 57 nested inside source region 43, etc. Openings in a layer of dielectric material 63 expose portions of the source/drain diffusion regions to form silicide 64. (See Abstract; col. 5, lines 39-67; and Figures 7 and 15 of Cheng).

Applicant's independent Claims 1 and 6, as amended herein, recite a semiconductor device where at least one heavily doped second drain and source diffusion layer has an outer lateral dimension along a surface of the semiconductor substrate in a vertical direction, and the sidewall offset is formed to have an outer edge which is at approximately the outer lateral dimension of the at least one heavily doped second drain and source diffusion layer. For purposes of example, Applicant refers to Figure 3 of the originally filed specification which includes a gate electrode 52 having a sidewall 53 and a sidewall offset 54. Heavily doped source and drain diffusion layers 65 and 66 are illustrated as having an outer lateral dimension in a vertical direction and the outer edge of the sidewall 54 is illustrated as having an outer edge which is approximately at the outer lateral dimension of diffusion layers 65 and 66.

Figure 15 of Cheng includes lightly doped source and drain regions 77' and 78', heavily doped source and drain diffusion layers 82' and 84' and the sidewall 66. The sidewall 66 is illustrated as having an outer edge which extends further along the substrate surface than the portions 82' and 84' located at the substrate surface. Figure 7 of Cheng similarly illustrates sidewall 66 extending further along the substrate surface than the portions 57 and 58.

Thus, Applicant respectfully submits that Cheng does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,316,977 to Kunishima et al. (hereinafter "Kunishima") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent Claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 5, 7, 11, 21 and 23 depend therefrom.

Kunishima discloses a method of manufacturing a semiconductor device comprising metal silicide. The Kunishima reference is cited by the Office Action as disclosing a silicide layer comprising titanium silicide, using a semiconductor device as a CMOS device, and a sidewall entirely covering the gate electrode.

Applicant respectfully submits that Kunishima fails to overcome the above-noted deficiencies of the Cheng reference with respect to Applicant's claimed invention. Kunishima does not disclose the configuration of a sidewall offset and heavily doped source and drain diffusion layers as set forth in Applicant's claims. As seen in Figure 3B of Kunishima, Kunishima discloses only a shallow diffusion layer 17, does not disclose a sidewall offset, and accordingly, does not disclose or suggest the above-referenced recited features of Claims 1 and 6

regarding an outer lateral dimension of a heavily doped second source and drain diffusion layer and an outer edge of a sidewall offset. Accordingly, Applicant respectfully submits that neither Kunishima nor Cheng, taken alone or in any combination, teach or fairly the above noted features as claimed by Applicant. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of Claims 20 and 22 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of U.S. Patent No. 5,439,835 to Gonzalez (hereinafter "Gonzalez") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

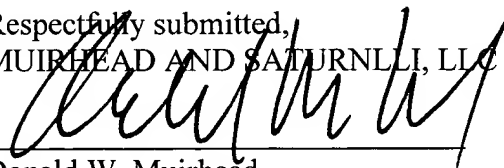
The features of independent claims 1 and 6 are discussed above with respect to the Cheng reference. Claims 20 and 22 depend therefrom.

Applicant respectfully submits that Gonzalez does not overcome the above-noted deficiencies of Cheng with respect to the Applicant's presently claimed invention. Gonzalez discloses a gate electrode, sidewall and sidewall offset and drain and source regions (see, for example, Figures 7-9 of Gonzalez), but the sidewall of Gonzalez below which are positioned multiple drain and source regions does not include a sidewall offset. Further, as seen for example in Figures 8 and 9, Gonzalez's N-implant region 81 has a portion under a sidewall; however the region disposed at the semiconductor substrate surface further extends laterally along the substrate surface beyond the sidewall. Thus, Gonzalez neither discloses nor suggests the above-referenced recited features of Claims 1 and 6 regarding an outer lateral dimension of a heavily doped second source and drain diffusion layer and an outer edge of a sidewall offset.

Accordingly, Applicant respectfully submits that Gonzalez and Cheng, taken alone or in any combination, do not teach or suggest at least the above features as claimed by Applicant and thus Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,  
MUIRHEAD AND SATURNELLI, LLC



Donald W. Muirhead  
Registration No. 33,978

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Muirhead and Saturnelli, LLC  
200 Friberg Parkway  
Suite 1001  
Westborough, MA 01581  
Phone: (508) 898-8601  
Fax: (508) 898-8602